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METALLIZATION OF HIGH ASPECT RATIO, OUT OF PLANE STRUCTURES

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Abstract **- This work is dedicated to developing a novel three dimensional structure for electrochemical measurements in neuronal studies. The final prototype will allow not only for the study and culture on chip of neuronal cells, but also of brain tissue.**

The use of out-of-plane electrodes instead of planar ones increases the sensitivity of the system and increases the signal-to-noise ratio in the recorded signals, due to the higher availability of surface area.

The main bottleneck of the out-of-plane electrode fabrication lies in the metallization process for transforming them into active electrodes, since the coverage of the side walls of almost vertical pillars is not trivial by standard processes in a clean room facility. This paper will discuss the different steps taken towards this goal and present the results that we have obtained so far.

1. INTRODUCTION

Electrical potential measurements on cells have provided a very sharp picture of neuronal activity at a single cell level. The introduction of microelectrode arrays 30 years ago made the repeated simultaneous recording from multiple sites in a non-invasive manner possible.

As reported, out of plane electrodes improve the signal to noise ratio in the recorded potentials [1], and seem to be the trend for solutions in this area. Namely, carbon nanotubes, nanowires, and three dimensional electrodes fabricated by clean room processes mark the lead in the field[2-5].

Several neurotransmitters, such as dopamine or glutamate, can be detected electrochemically. But to monitor neurotransmission, chemical sensors must be fast enough, since neurotransmitter lifetimes are very short once released by the cells [6]

In our work we propose the fabrication of a novel three dimensional electrode array, where high aspect ratio structures have been designed for an electrochemical environment, where reduction and oxidation of the species in solution give the cues to the processes taking place in the neurons. The integration of the counter electrode with surrounding active electrodes (Fig. 1) is expected to translate into a signal enhancement, since less ions of the ongoing reactions would diffuse back into the bulk solution; this design helps to obtain a homogeneous distribution of current density among them and thus makes the sensor system more reliable against disturbances such as bubbles in the microfluidic system for cell culturing or inhomogeneous directionality of the input signal.

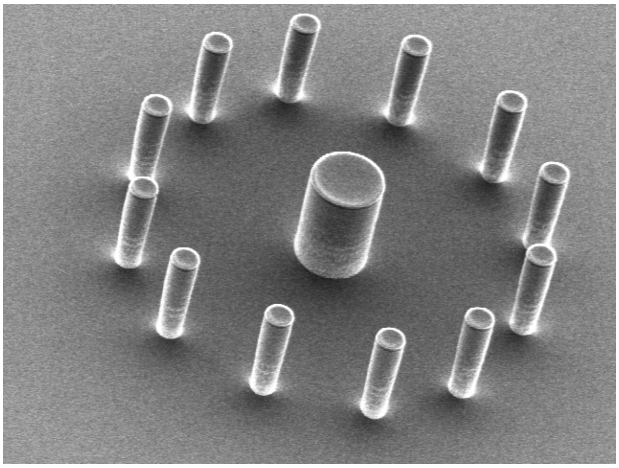


Fig. 1: SEM picture of one electrode layout in the array. The counter electrode lies in the center, surrounded by the active electrodes.

The system is also intended to be used in brain tissue slices studies, since the electrode height (in the order of 100 μm) is big enough to penetrate the dead cell layers at the surface of the brain slice, thus reducing the distance to the active cells and increasing the signal.

The electrodes are fabricated in silicon and their walls are completely covered by a thin metal layer that acts as the conductor element.

A major drawback in the fabrication of out-of plane structures as tall as in our system, around 100 μm, is the metallization step, where they become active electrodes. The technical challenge resides into covering the almost vertical walls of the pillars.

2. FABRICATION PROCESS

The main steps followed in the fabrication process are described in Fig. 2. The first step is to define by photolithography the areas of the silicon that will be etched; this is done by spinning a thick resist of 4 μm on the wafer and then exposing and developing it to obtain the mask features to define the area of what will be the electrodes. The wafer is then dry etched in an Advanced Silicon Etcher (ASE) equipment, a STS MESC Multiplex ICP, and thus we obtain the pillar structures. A posterior layer of silicon nitride is deposited in a Low Pressure Chemical Vapor Deposition (LPCVD) furnace to isolate

each electrode from the rest. Finally, the pillars become active electrodes by metallization of their surface.

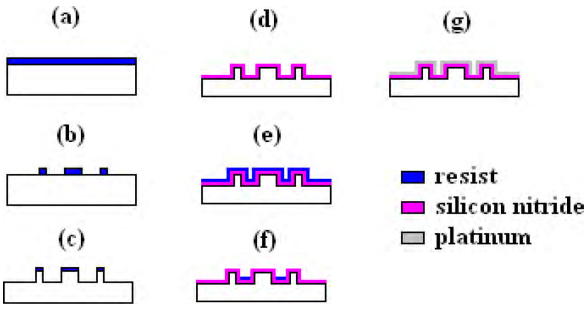


Fig. 2. Fabrication procedure for out of plane electrodes. (a) and (b) are typical steps to define by photolithography a pattern on a silicon wafer; (c), creation of the pillars after etching; (d) isolation of electrode structures by growth of a silicon nitride; (e) and (f) show a second photolithography step to define wiring and electrodes areas for the final (g) metallization of electrodes.

Metallization

Procedures for metallization of high aspect ratio and out of plane structures are not commonly mentioned in literature. This is due to the fact that there is not a perfect viable solution for this problem. The major concern is the quality of step coverage at the electrode sites.

There are three steps necessary in the metallization of the electrodes: a negative photolithography process in which the wires and electrode sites are defined; metal deposition in itself, and lift off of the remaining resist and non desired metal areas.

In regards to the photolithography process, one of the main issues in our particular design is the existence of a hollow shape that will form the final chip area, a 2x2 cm square in whose center the array of electrodes lies. This hollow shape was included in the design for different reasons, but was mainly intended to act as a stopper of the mask when performing a hard contact photolithography process. The mask with the desired patterns is attached by vacuum to the surface onto which those patterns are to be transfered. If the hole was not designed, the hard contact of the mask against the silicon wafer would systematically destroy the pillar-electrodes that stand out from the substrate. Yet, this hollow feature hinders a good transfer of the patterns onto the substrate, since there is a factual distance in the order of 100 µm (the hole is etched during the same process as the pillars) from the mask to the substrate.

Also, the out-of-plane structures hinder an even spun of the resist and block the light during the process of exposure. We have studied several distances between electrodes and different thicknesses (1.5. 2.2 and 4.2 µm) of the resist deposited on the wafer, and have concluded that for an optimal resist spread, a minimum of 250 µm pitch (see Fig. 3) is necessary. The different thicknesses used in the experiments didn't show any relevant improvement in the results.

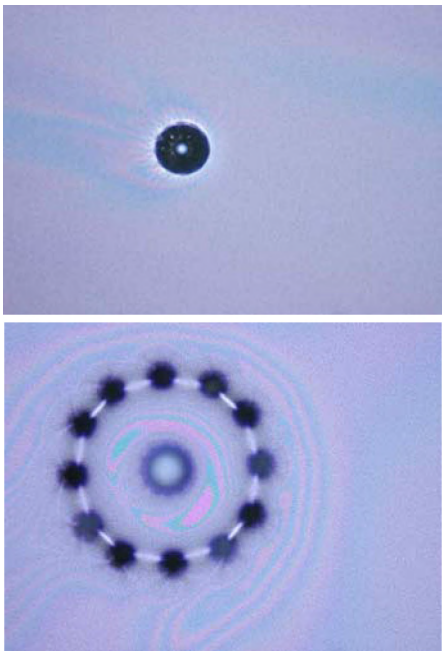


Fig. 3. Spun resist (1.5 µm) on (top) the site of a 30 µm electrode surrounded by sacrificial pillars at a pitch of 100 µm and (bottom) a 50 µm electrode with surrounding pillars at a pitch of 250 µm.

In addition, the effect of the slack distance between mask and substrate translates into poor definition of the wires on the substrate (Fig. 4, top), seeing both over- and underexposure at different locations.

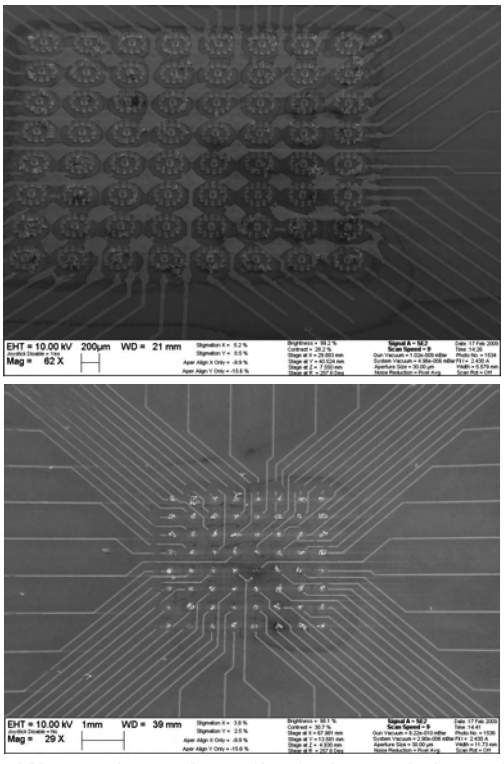


Fig. 4. Different views of metalized wires and electrode sites

For the metallization step itself, Pt was the material of choice; the reasons behind this decision lie on the fact that it is biocompatible and durable in electrochemical environments, and thus it is a suitable candidate for our chip. The metal was deposited on the wafer with a Physical Vapor Deposition (PVD) process carried out in a magnetron sputtering machine for 299 seconds. This process provides good step coverage, which is critical for reliability of electrical conductivity in the electrodes.

After a lift-off step of the previously patterned photoresist, the electrodes and wiring for those structures with the optimal pitch appear on the surface of the wafer, as shown in Fig. 4.

Fig. 5 shows the first results from the metallization process. The picture shows some debris remaining after the lift-off process (top left corner and bottom right), but it can be observed, that the majority of the wall surface remains uncovered after the deposition. This result was confirmed by obtaining an x-ray spectrum in the SEM. Although spectrum 2 shows some trace of Pt, it is not enough to assure proper conductivity, and the rest of data is in agreement to conclude the non-existence of a metal layer on the walls. In order to obtain a better coverage at the side walls of the pillars, we used a custom-made holder to tilt the wafer inside the vacuum chamber of the sputtering system. This has allowed us to obtain very promising results, as it can be confirmed by comparing Fig. 5 and Fig. 6. Although the coverage of the sidewalls is not fully accomplished, the improvement is obvious.

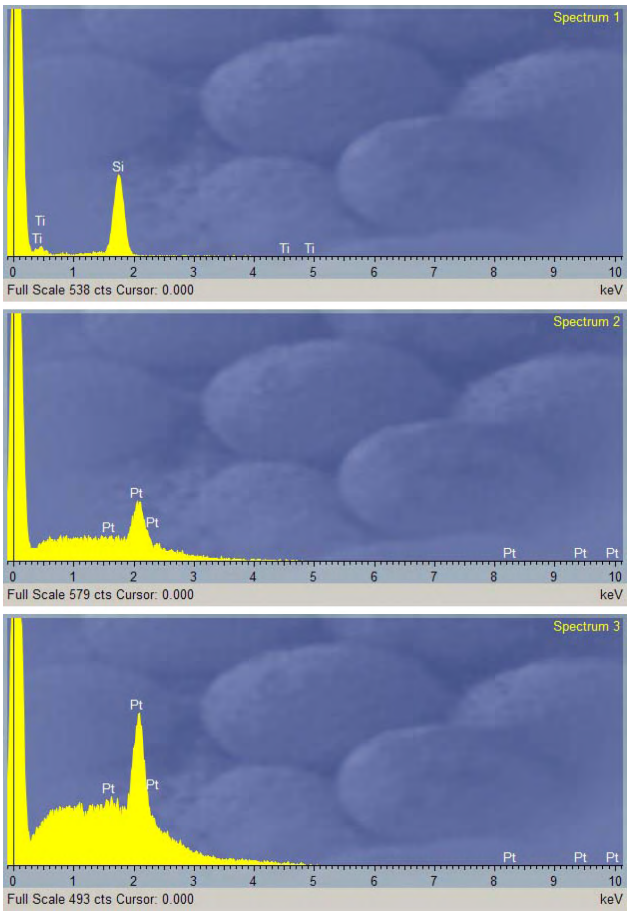
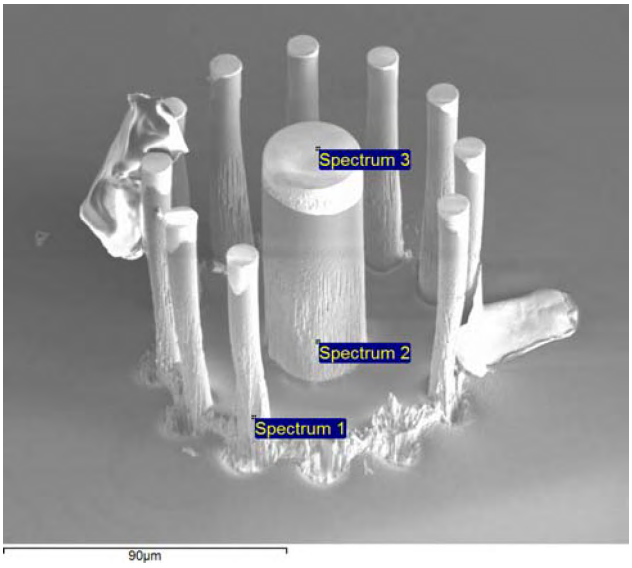


Fig. 5. Metallization with Pt during 299 s and spectra taken at different points of the structures.



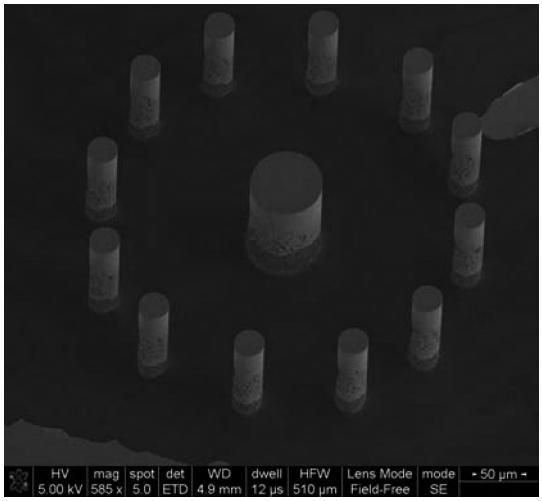


Fig. 6. Pt coverage after tilting the wafer in the vacuum chamber

3. RESULTS AND CONCLUSIONS

Several technical issues arise in the presence of different planes when it comes to photolithographic processes and metallization. The different height between the top of the electrodes and the surface of the wafer, together with the density of the electrodes interfere with a perfect trans-

fer of the desired pattern onto the wafer. We have found that with a pitch of 250 μm it is possible to obtain reasonably good wafer coverage.

Although the metallization process requires some optimization, the first results obtained from tilting the wafer inside the vacuum chamber when performing the metal sputtering are encouraging. Moreover, our structures will be optimized in order to obtain sharp tips, which will allow for a sufficient metallization of the walls when using the tilting method.

Furthermore, we are carrying ongoing experiments using a shadow mask for the metal deposition, which would allow us to avoid the photolithography step and thus the imprecision present in this process. The results from these last experiments will be shown in short.

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